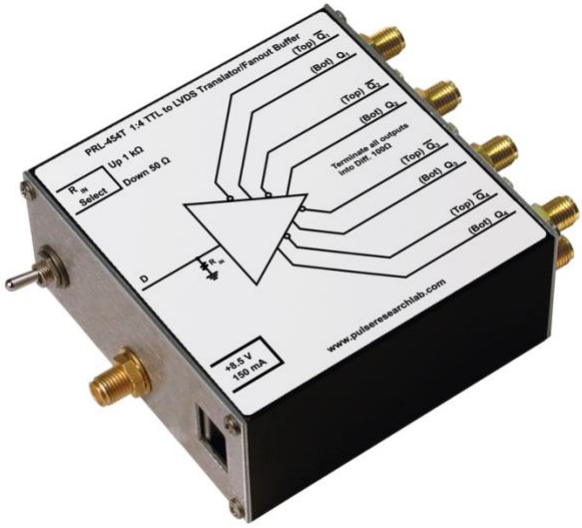
PRL-454T 1:4 TTL TO LVDS TRANSLATOR AND FANOUT BUFFER

APPLICATIONS

- Converting TTL Input to LVDS Outputs
- Conversion of Single-Ended TTL Signals to Differential Signals for Driving Long Lines
- Distributing Clock/Data Signals
- High Speed Digital Communications Systems Testing
- Satellite Telemetry/Ground Station System Integration

FEATURES

- f_{max} > 400 MHz for 50 Ω input and > 250 MHz for 1 k Ω input
- 1 kΩ or 50 Ω TTL Input, selectable by a switch
- 500 ps Typical Output Rise & Fall Times
- 4 LVDS Outputs for Driving 50 Ohm Cables into 100 Ω Floating Loads
- 300 ps Channel to Channel skew, typical
- SMA I/O Connectors
- Operates from single +8 to +12 VDC power supply with only 150 mA max.
- Self-contained 1.3 x 2.9 x 2.9-in. unit includes ±8.5 V/1.8 A AC/DC Adapter



PRL-454T-SMA, 1:4 TTL to LVDS Translator and Fanout Buffer

DESCRIPTION

The PRL-454T-SMA is a 1:4 digital signal fanout buffer and level translator with one TTL input and four LVDS outputs.

The TTL input has a 1 kΩ or 50 Ω input impedance, selectable by a toggle switch. The 1 kΩ input setting is used most often for receiving signals from digital I/O boards. These DIO boards are generally not designed for driving 50 Ω loads. For this type of application, it is recommended that the interconnecting cable length be limited to no more than 18 inches. For applications exceeding this length, pre-buffering the TTL signal with a PRL-444, High Input Impedance Line Driver, may be required.

When switched to the 50 Ω input position, f_{max} can be increased beyond 400 MHz. Since very few affordable TTL clock generators can run beyond 250 MHz, we recommend that the PRL-177A-500 be used for testing the PRL-454T-SMA. The PRL-454T-SMA has a 5 V tolerant input and can be driven by the PRL-177A-500 directly.

The PRL-454T-SMA is housed in a 1.3 x 2.9 x 2.9-in. extruded aluminum enclosure and is supplied with a ±9.0 V/±1.8 A AC/DC Adapter. The PRL-454T-SMA may also be ordered without the power supply as part number PRL-454T-SMA-OEM. A maximum of four units can share the included PRL-760E AC/DC adapter using additional units of cable #88000102-4. If mounting is desired, a pair of the #35001420 mounting brackets can accommodate any two PRL modules of the same length. Please refer to the Accessories section of www.pulseresearchlab.com for more detail.

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*SPECIFICATIONS (0° C ≤ T_A ≤ 35° C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into floating 100 Ω loads.

SYMBOL	PARAMETER	Min	Typ	Max	UNIT
R_{IN1}	Input Resistance Low Range	49.5	50.0	50.5	Ω
R_{IN2}	Input Resistance High Range	990	1000	1010	Ω
R_{out}	Output Resistance (current source)		N/A		Ω
V_{IL}	TTL Input Low Level	-0.5	0.0	0.8	V
V_{IH}	TTL Input High Level	1.6	2.0	5.0	V
V_{OL}	LVDS Output Low Level		1.05		V
V_{OH}	LVDS Output High Level		1.35		V
V_{CMO}	Output Common mode voltage[1]		1.20		
I_{DC}	DC Input Current			150	mA
V_{DC}	DC Input Voltage	7.5	8.5	12.0	V
V_{AC1}	AC/DC Adapter Input Voltage, 120	103	115	127	V
V_{AC2}	AC/DC Adapter Input Voltage, 220	206	220	254	V
t_{PLH}	Propagation Delay to output ↑		2.7		ns
t_{PHL}	Propagation Delay to output ↓		2.7		ns
t_r/t_f	Rise/Fall Times (10%-90%)		500	700	ps
t_{SKEW}	Skew between any 2 outputs		300	550	ps
f_{max1}	Max Clock Frequency, R_{IN} = 50 Ω	350	400		MHz
f_{max2}	Max Clock Frequency, R_{IN} = 1 kΩ	200	250		MHz
	Size	1.3 x 2.9 x 2.9			in
	Weight	5			Oz
	Shipping Weight	4			lb

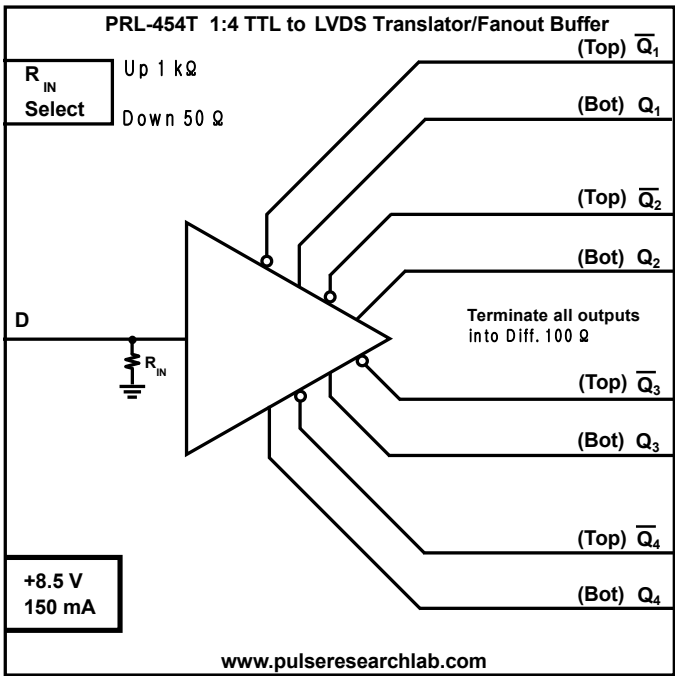


Fig.1: PRL-454T Block Diagram

Notes:

1. V_{CMO} = (V_{OH}+V_{OL})/2
2. Rise and Fall times are measured using a PRL-425NCML LVDS receiver and a PRL-860D-SMA inline signal monitor
3. f_{max} is measured using the PRL-177A-500 as the driver and the PRL-425NCML as the as the receiver.

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