PRL-4540, 4 Channel TTL/BNC TO Differential TTL Logic Translator System

APPLICATIONS

- Translating TTL signals to Differential TTL signals
- Clock/Trigger Distribution
- High Speed Digital Communications System Testing



PRL-4540 Front View



PRL-4540, Rear View

FEATURES

- f_{max} > 200 MHz, 250 MHz typical
- 1.2 ns Typical Output Rise & Fall Times
- Four 50 Ω Single-ended TTL BNC Inputs
- Four Differential TTL Outputs on D38999/20FC35SN
- DC Coupled I/Os
- Self-contained, 1U, 19" rackmount enclosure
- 120 - 240 VAC auto-switching power supply

DESCRIPTION

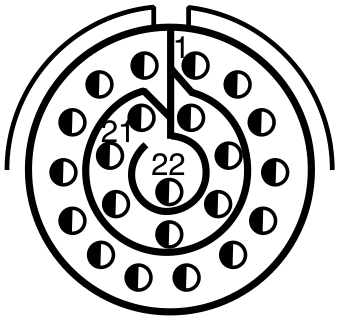
The PRL-4540 is an 4 channel logic level translator system with four single-ended, 50 Ohm TTL inputs on BNC connectors and four differential TTL output pairs on a mass-terminated D38999/20FC35SN connector. It is designed for translation of high-speed clock and trigger signals.

The TTL inputs have a fixed at 50 Ω impedance, but require only 1.5 V to trigger. A set of internal toggle switch can reduce this further to 1.0 V. The differential TTL outputs are designed to drive twisted pair cabling into either 100 Ω/124 Ω floating loads or 50 Ω loads to Ground. The outputs of the PRL-4540 can toggle at clock rates greater than 250 MHz, typical. All I/Os are DC coupled.

The PRL-4540 is equivalent to 2 units of the PRL-420TD, 2 Channel TTL to Differential TTL Translator, integrated into a 1U chassis with an internal, auto-switching 120 VAC/240 VAC power supply, and an internal 88001641-2-C00x breakout cable with mass-terminated output connector.

Pinout C002:

Pin	Signal	Coax Connection
1	CH1(+)	Sub cable 1A signal
2	CH1(-)	Sub cable 1B signal
3		Sub cable 1 shield
4	CH2(+)	Sub cable 2A signal
5	CH2(-)	Sub cable 2B signal
6		Sub cable 2 shield
7	CH3(+)	Sub cable 3A signal
8	CH3(-)	Sub cable 3B signal
9		Sub cable 3 shield
10	CH4(+)	Sub cable 4A signal
11	CH4(-)	Sub cable 4B signal
12		Sub cable 4 shield



20FC35SN, Pin Mating Face

The PRL-4540 may be with ordered custom pinout on the 20FC35SN connector and/or with a custom silkscreen, which case the model would be identified as PRL-4540-C00x, where each configuration has a unique suffix, but all PRL-4540 units will have the same form factor and electrical function.

Use matching breakout cable 88001642-6-C00x, 26FC35PN to 8 x SMA-M, for testing.

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*SPECIFICATIONS (0° C ≤ T_A ≤ 35° C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into 50 Ω.

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
R_{IN}	Input Resistance	49.5	50.0	50.5	Ω	
R_{OUT}	Differential Output Resistance	99	100	101	Ω	
V_{TOSH}	Input Threshold Voltage (High)	1.4	1.5	1.6	V	Internal switches Up (Default)
V_{TOSL}	Input Threshold Voltage (Low)	0.9	1.0	1.1	V	Internal switches Down
V_{IL}	TTL Input Low Level	-0.5	0	0.5	V	
V_{IH}	TTL Input High Level	1.8	2.0	5.0	V	
V_{OL}	Differential TTL Output Low Level	-0.1	0.0	0.5	V	50 Ω load
V_{OH}	Differential TTL High Level	2.0	2.5	2.6	V	50 Ω load
I_{DC1}	DC Input Current, +8.5 V		340	360	mA	Each internal unit
I_{DC2}	DC Input Current, -8.5 V	-360	-340		mA	Each internal unit
V_{DC1}	DC Input Voltage, +8.5 V	7.5	8.5	12.0	V	Internal Units
V_{DC2}	DC Input Voltage, -8.5 V	-12.0	-8.5	-7.5	V	Internal Units
V_{AC}	AC Input Voltage	100		264	V	50/60 Hz auto-switching
T_{PLH}	Propagation Delay to output ↑		7		ns	
T_{PHL}	Propagation Delay to output ↓		7		ns	
t_r/t_f	Rise/Fall Times (10%-90%)		1.0	1.4	ns	Note (1)
T_{SKEW}	Skew between any 2 outputs		150	400	ps	
f_{max}	Max Clock Frequency	200	250		MHz	
	Size (W x H x D)	18.95 x 1.75 x 13.10			in.	11.78" D from rack face
	Weight	5.5			lb	

(1). The output rise and fall times are measured with both the Q and $\overline{Q}$ outputs terminated into 50 Ω.

A block diagram of one PRL-420TD subassembly is shown in Fig. 1, and a block diagram of the system is shown in Fig. 2.

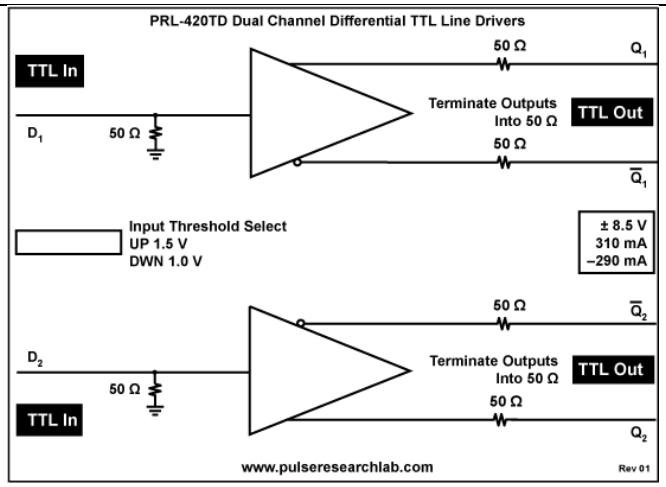


Fig. 1: PRL-420TD Block Diagram

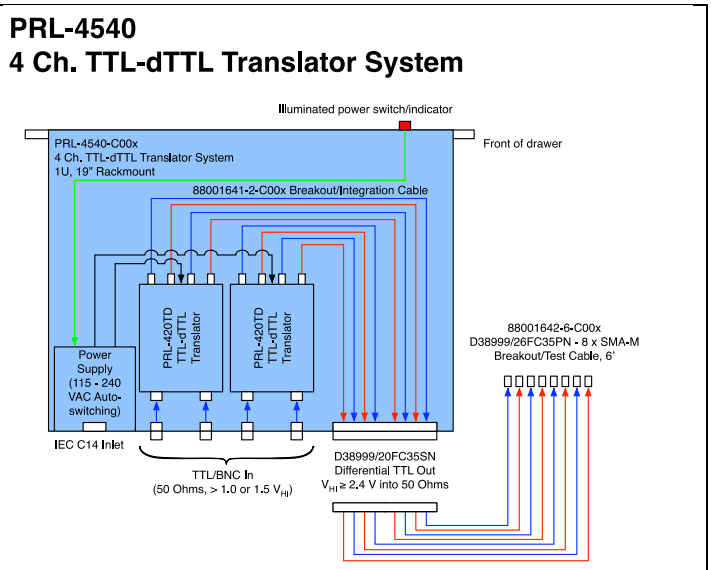


Fig. 2: PRL-4540 Block Diagram

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