# PRL-4533 1:8 DIFFERENTIAL FANOUT BUFFER SYSTEM, DIFFERENTIAL / TTL INPUTS, 50 Ω BACK-TERMINATED TTL OUTPUTS

## APPLICATIONS

- Long Line Driver/Level Translator
- Reference Clock Distribution/Translation
- 1 PPS/IRIG-B Signal Distribution
- Test and System Integration



**PRL-4533 Front View**



**PRL-4533 Rear View**

## FEATURES

- 1:8 Fanout with Complementary TTL Outputs
- Channel-to-channel Skew < 500 ps
- $t_R$= 1.4 ns Typ. @ 2.5 V Output into 50 Ω
- Back-terminated 50 Ω Outputs Drive Long Lines into 50 Ω or Unterminated Loads
- TTL and Universal Differential Inputs (logically ORed)
- Universal Differential Input compatible with LVDS, RS-422, Differential TTL, NECL, or LVPECL signals
- Standard 19-in. Rack-Mount Chassis with optional slide rails

## GENERAL DESCRIPTION

The PRL-4533 is a 1:8 differential fanout buffer system with 8 complementary 50 Ω back-terminated TTL outputs and two inputs. The single-ended TTL input has a selectable 50 Ω or 1 KΩ to ground termination. The Universal Differential input can be driven by LVDS, RS-422, Differential TTL, NECL, or LVPECL signals with source bias. The TTL and Differential inputs are logically ORed; therefore a Hi level applied to either input can be used as a gate signal.

The input resistance of the TTL input can be selected to be either 50 Ω or 1 KΩ by a toggle switch. The 1 KΩ input is desirable when interfacing with low power circuits. The TTL input threshold voltage is 1.0 V minimum. When over-driven, the input voltage to the internal circuit is limited to 3.5 V through a current limiting 25 Ω series resistor.

The Universal Differential input has a floating 100 Ω termination and requires a minimum differential input swing of 200 mV, with an input Common Mode Range of -2.4 V to +4.0 V.

The TTL output swing is typically 0-2.5 V into 50 Ω or 0-5.0 V into high impedance. All outputs are independently buffered, so they can be used single-ended or as a complementary pair, and unused complements or outputs do not require termination.

All I/Os are DC coupled, with BNC inputs at the front of the unit and BNC outputs at the rear of the unit. The PRL-4533 is housed in a standard 19-in. rack-mountable enclosure with optional slide rails, powered by an internal auto-switching power supply suitable for 120/240 VAC, 50-60 Hz operation.

Models with a suffix, e.g. PRL-4533-C001, indicate a unit with a customer-specific silkscreen or labeling, but all PRL-4533 models are functionally equivalent.

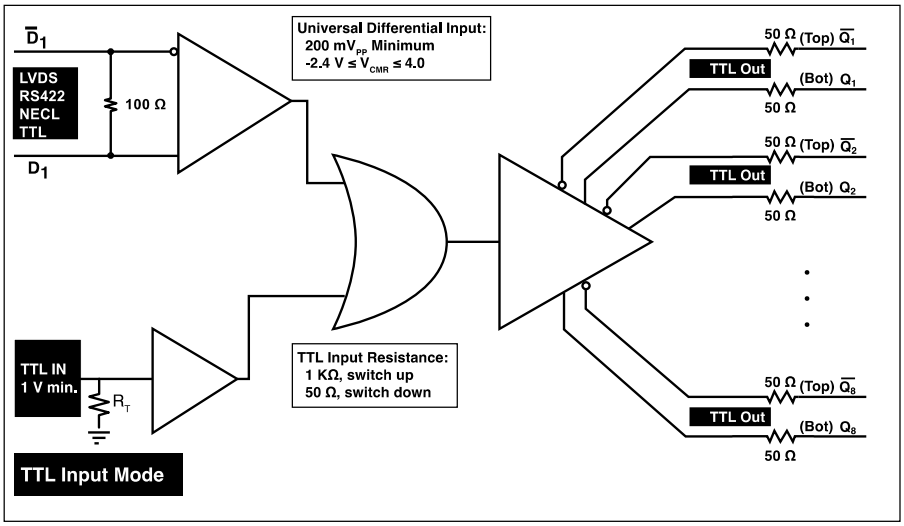


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## *SPECIFICATIONS (0 °C ≤ $T_A$ ≤ 35 °C)

Unless otherwise specified, dynamic measurements are made with all rear-panel outputs terminated into 50 Ω.

| SYMBOL | PARAMETER | Min | Typ | Max | UNIT | Comment |
|---|---|---|---|---|---|---|
| $R_{inD}$ | Differential Input Resistance | 95 | 100 | 105 | Ω | |
| $R_{inC}$ | Common Mode Input Resistance, Diff. Input | | 5K | | Ω | |
| $V_{CMV}$ | Input Common Mode Voltage, Diff. Input | -2.4 | | +4.0 | V | |
| $R_{T2-1}$ | Input Resistance, TTL 50 Ω | 49 | 50 | 51 | Ω | |
| $R_{T2-2}$ | Input Resistance, TTL 1 KΩ | 0.95 | 1.00 | 1.05 | KΩ | |
| $V_{IH1}$ | TTL Input Hi Level | 1.0 | | 5.0 | V | Internally limited to 3.5 V |
| $V_{IL1}$ | TTL Input Lo Level | -0.5 | | 0.5 | V | |
| $R_{OUT}$ | Output Resistance | 49.5 | 50.0 | 50.5 | Ω | |
| $V_{OH1}$ | Output High Level | 2.2 | 2.5 | 2.6 | V | $R_{LOAD}$ = 50 Ω |
| $V_{OH2}$ | Output High Level | 4.4 | 5.0 | 5.2 | V | $R_{LOAD}$ = 1 MΩ |
| $V_{OL}$ | Output Low Level | -0.25 | 0.00 | 0.25 | V | |
| $V_{AC}$ | AC Input Voltage | 108 | | 254 | V | |
| $V_{VA}$ | AC Input Power | | 40 | 45 | VA | |
| $T_{PROP1}$ | Prop. Delay to Output ↑, Diff. Input | | 6.0 | | ns | See Notes 1, 2 |
| $T_{PROP2}$ | Prop. Delay to Output ↑, TTL Input, 50 Ω | | 6.5 | | ns | See Notes 1, 2 |
| $T_R$ | Rise Time (10%-90%) | | 1.4 | 2.0 | ns | |
| $T_F$ | Fall Time (10%-90%) | | 1.4 | 2.0 | ns | |
| $T_{SKEW1}$ | Ch./Ch. skew between any 2 True Outputs | | | 500 | ps | See Notes 1, 2 |
| $F_{MAX1}$ | Max Clock Frequency, Differential Input | 150 | 175 | | MHz | |
| $F_{MAX2}$ | Max Clock Frequency, TTL Input | 100 | 125 | | MHz | |
| | Size | 19.0"W x 3.5"H x 16.5"D | | | in | Excluding slide rails |
| | Weight | 13 | | | lbs | |




**PRL-4533 Block Diagram (simplified)**

**Notes:**

1. Skew measurements valid when using same input logic level. TTL-input measurements made with TTL input set to 50 Ω.
2. $T_{PROP}$ and $T_{SKEW}$ measurements made via PRL-8506 Test Mux, which provides 50 MHz input clocks in NECL and TTL logic as well as delay-matched NECL and TTL reference timing paths.




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