

PRL-4520, 2 x 1:8 LOGIC TRANSLATOR/FANOUT BUFFER, LVDS INPUTS, TTL OUTPUTS

APPLICATIONS

- Translating LVDS signals to TTL signals
- TTL/CMOS Clock/Trigger Distribution
- Synchronous Clocking/ Triggering of Dalsa X64 Xcelera-HS PX8 and similar framegrabbers
- High Speed Digital Communications System Testing

FEATURES

- $f_{\max} > 80$ MHz, 90 MHz typical
- Drives 100 ft of cable @ 50 MHz
- 1.8 ns Typical Output Rise & Fall Times
- 2.5 V into 50 Ω Typical
- 2 x 100 Ω Triax LVDS Inputs
- 2 x Eight In-phase 50 Ω TTL SMA Outputs
- DC Coupled I/Os
- Valid signal LED indicators
- Self-contained 1U, 19" rackmount enclosure



PRL-4520-C001, Front View



PRL-4520-C001, Rear View

DESCRIPTION

The PRL-4520 is 2 x 1:8 logic level translator and fanout buffer/pulse distribution amplifier with two LVDS Triax inputs and sixteen 50 Ω TTL/SMA outputs. It is designed for translation and distribution of high-speed clock and trigger signal to multiple loads via long lines, especially the synchronous clocking/triggering of Dalsa X64 Xcelera-HS PX8 and similar framegrabbers. The 50 Ω back-terminated outputs can drive long lines with or without 50 Ω load terminations. With 50 Ω load terminations, however, all outputs of the PRL-4520 can drive 100 ft of 50 Ω cables at clock rates greater than 50 MHz.

Each bank of the PRL-4520 has a differential 100 Ω LVDS Triax input and eight 50 Ω back terminated TTL SMA outputs, which typically deliver 2.5 V into 50 Ω or 5.0 V into Hi-Z loads. An additional TTL output is wired to an LED driver to provide a valid signal indicator for each channel, shown as Clock and Trigger in the photo above. All I/Os are DC coupled. An equivalent circuit of the PRL-4520 LVDS input is shown in Fig. 1, and the internal signal fanout and distribution block diagram is shown in Fig. 2.

The PRL-4520 is housed in a standard 1U, 19" rackmount enclosure. External 8V/12V, 2A DC power is required.

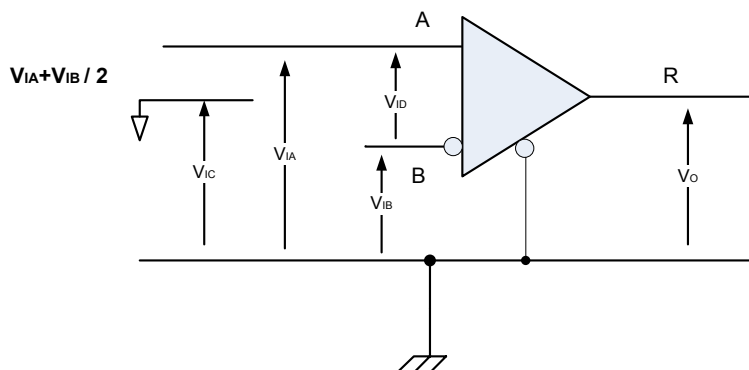


Fig. 1: RECEIVER VOLTAGE DEFINITION

The PRL-4520 may be with ordered with a custom silkscreen, which case the model would be identified as PRL-4520-C00x, where each configuration has a unique suffix, but all PRL-4520 units will have the same form factor and electrical function.

*SPECIFICATIONS (0° C ≤ T_A ≤ 35° C)

Unless otherwise specified, dynamic measurements are made with LVDS 100 Ω input driven by complementary signal and all outputs terminated into 50 Ω.

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
R _{IN}	Input Resistance	95	100	105	Ω	Floating differential
R _{OUT}	Output Resistance		50		Ω	
V _{IA}	Non-Inverting Input	0		2.5	V	Fig. 1
V _{IB}	Inverting Input	0		2.5	V	Fig. 1
V _{ID}	Differential Input	35	100		mV	Fig. 1
V _{IC}	Common Mode Voltage	0	1.2	3.0		V _{IC} =(V _{IA} +V _{IB})/2
V _{OL}	TTL Output Low Level	0.0	0.25	0.5	V	R _L =50 Ω
V _{OH1}	TTL Output High Level	2.2	2.5		V	R _L =50 Ω @ DC
V _{OH2}	TTL Output High Level	4.4	5.0		V	R _L =1 MΩ @ DC
I _{DC1}	DC Input Current		1256		mA	f=85 MHz, 8 outputs loaded/bank
I _{DC2}	DC Input Current		1354		mA	f=85 MHz, 10 outputs loaded
I _{DC3}	DC Input Current		1080		mA	f=50 MHz, 10 outputs loaded
V _{DC}	DC Input Voltage	8.0	8.5	12.0	V	
T _{PLH}	Propagation Delay to output ↑		17	21	ns	
t _r	Rise Time (10%-90%)		1.8	2.5	ns	
t _f	Fall Time (10%-90%)		1.5	2.5	ns	
T _{SKW1}	Skew between any 2 outputs		0.5	1.5	ns	Within same bank
T _{SKW2}	Skew between any 2 outputs		1.0	3.0	ns	Within same unit
F _{MAX1}	Max. Clock Frequency ⁽²⁾	80	90		MHz	Driven by PRL-426NTR
F _{MAX2}	Max. Clock Frequency		50			RG58C/U, cable length = 100 ft
PW _{MIN1}	Minimum Pulse Width		4		ns	↑ Input
PW _{MIN2}	Minimum Pulse Width		6		ns	↓ Input
	DC input connector	TE/Amp 350778-1				Or equivalent
	Size (W x H x D)	18.95 x 1.75 x 10.5			in.	Depth from rack face
	Weight	1.5			lb.	

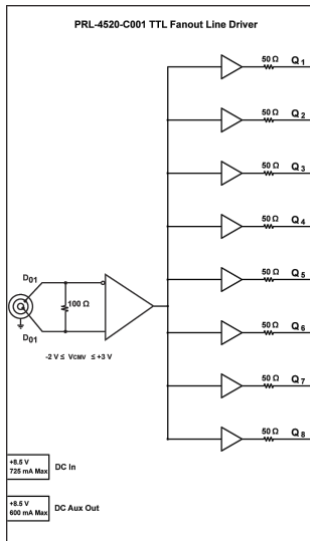


Fig. 2: PRL-4520, TTL Fanout
Block diagram

Notes:

(1) f_{MAX} should not exceed 100 MHz, otherwise damage of the unit due to overheating may result.

f_{MAX2} is measured by driving a PRL-4110 at the end of a 100 ft cable.

Block Diagram of single channel shown. Two identical channels are included in the unit.