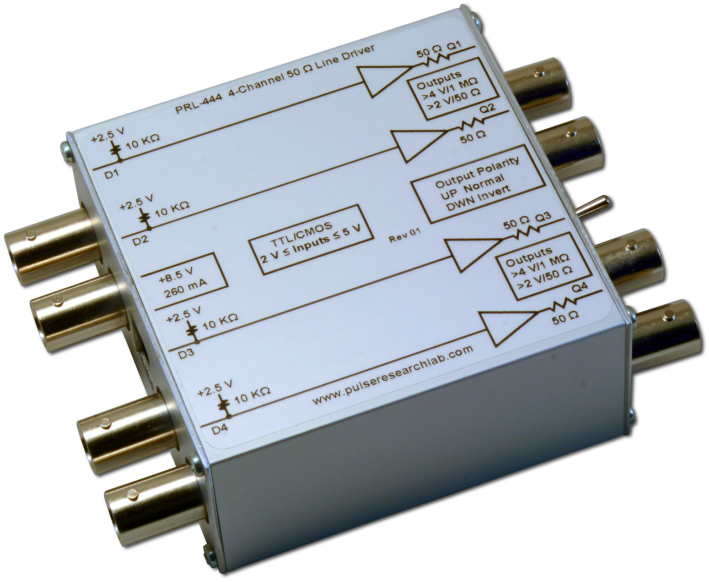
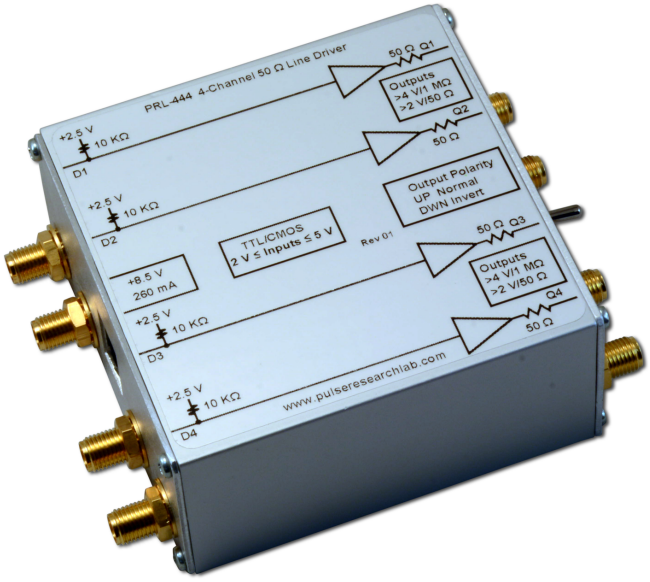
PRL-444 Four Channel High Input Impedance 50 Ω TTL Line Driver



PRL-444-BNC, 4 Channel TTL Line Driver



PRL-444-SMA, 4 Channel TTL Line Driver

APPLICATIONS

- Converting Conventional TTL/CMOS Outputs to 50 Ω TTL Outputs
- Long Line Drivers
- High Speed Digital Communications System Testing
- Basic Lab Tool
- HI/LO Logic Level Generation

FEATURES

- f_{max} > 70 MHz Normal/50MHz Invert
- Drives 100 ft of cable @ 50 MHz Normal
- 2ns Typical Output Rise & Fall Times
- Four independent TTL Compatible 10 kΩ Inputs
- Four independent 50 Ω TTL Outputs
- BNC or SMA I/O Connectors
- DC Coupled I/O's
- Self-contained 1.3 x 2.9 x 2.9-in. unit includes an AC/DC Adapter

DESCRIPTION

The PRL-444 is a four channel TTL/CMOS input, 50 Ω output TTL/CMOS Line Driver. It is intended for interfacing with computer I/O cards that have TTL outputs not suitable for driving 50 Ω lines. Each input has a 10 kΩ pulled up to 2.5V so that it can also be driven by open collector devices. The 50 Ω back-terminated outputs of the PRL-444 can drive long lines with or without 50 Ω load terminations. With 50 Ω load terminations, however, all outputs can drive 100 ft of 50 Ω cables at clock rates greater than 60 MHz.

If the inputs are left open, all outputs will go Hi, because the inputs are pulled up to +2.5V. All outputs can be set to the LO state, however, by either setting the polarity inverting switch to the down position or terminating all inputs to 2 kΩ or lower. The polarity inverting switch enables easy generation of four static Hi/Lo logic signals when the inputs are not driven.

The PRL-444 is housed in a 1.3 x 2.9 x 2.9-in. extruded aluminum enclosure and is supplied with a ±8.5 V/±1.4 A AC/DC Adapter. A maximum of four units can share a single AC/DC adapter using the PRL-730 or PRL-736 voltage distribution modules. If mounting is desired, a pair of the #35001420 mounting brackets can accommodate any two PRL modules of the same length. Please refer to the Accessories Section of the literature for more detail.

A block diagram showing the equivalent input and output circuits of the PRL-444 is shown in Fig. 1.

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SPECIFICATIONS* (0° C ≤ T_A ≤ 35°C)

Unless otherwise specified, dynamic measurements are made with all inputs and outputs terminated into 50 Ω

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
R_{in}	Input Resistance	9.9	10	10.1	kΩ	Pulled up to +2.5V
Rout	Output Resistance		50		Ω	
V_{IL}	TTL input Low Level	-0.5	0.0	0.5	V	
V_{IH}	TTL input High Level	2.0	2.4	5.0	V	
V_{OL}	TTL Output Low Level	0.0	0.25	0.5	V	R_L=50 Ω
V_{OH1}	TTL Output High Level	2.2	2.5		V	R_L=50 Ω @ DC
V_{OH2}	TTL Output High Level	4.4	5.0		V	R_L=1 MΩ @ DC
I_{DC1}	DC Input Currents		260	300	mA	f ≤ 75 MHz
I_{DC2}	DC Input Currents		220	250	mA	f =50 MHz sq. wave(1)
V_{DC}	DC Input Voltages	7.5	8.5	12	V	
V_{AC}	AC/DC Adaptor Input Voltage	103	115	127	V	
T_{PLH}	Propagation Delay to output ↑		15	20	ns	
T_{PHL}	Propagation Delay to output ↓		15	20	ns	
t_r	Rise Time (10%-90%)		2.2	3	ns	f =50 MHz sq. wave
t_f	Fall Time (10%-90%)		1.8	3	ns	f =50 MHz sq. wave
T_{SKEW}	Skew between any 2 outputs		900	1800	ps	f =50 MHz sq. wave
F_{max1}	Max. Clock Frequency Outputs set to Normal	70	80		MHz	RG58C/U Cable length =3 ft
F_{max2}	Max. Clock Frequency Outputs set to Invert	50	60		MHz	RG58C/U Cable length =3 ft
F_{max3}	Max. Clock Frequency(2) Outputs set to Normal	50	60		MHz	RG58C/U Cable length =100 ft
PWmin	Minimum Pulse Width		8		ns	↑ Input
PWmin	Minimum Pulse Width		8		ns	↓ Input
	Size	1.3 x 2.9 x 2.9			in.	
	Weight	5			Oz	

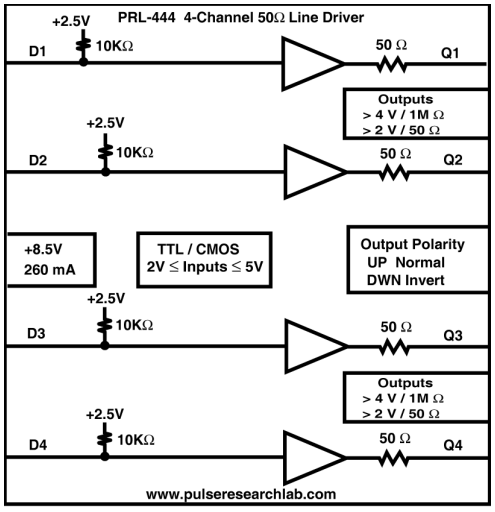


Fig. 1: PRL-444 Functional Block diagram

Notes:

(1). For sharing a single PRL-760C, ±8.5 V, ±1.8 A AC/DC adapter, the total current should not exceed 1.8 A.

(2). f_{MAX3} is measured by connecting a second PRL-444, with its input terminated into 50 Ω, at the end of the 100 ft cable.

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