

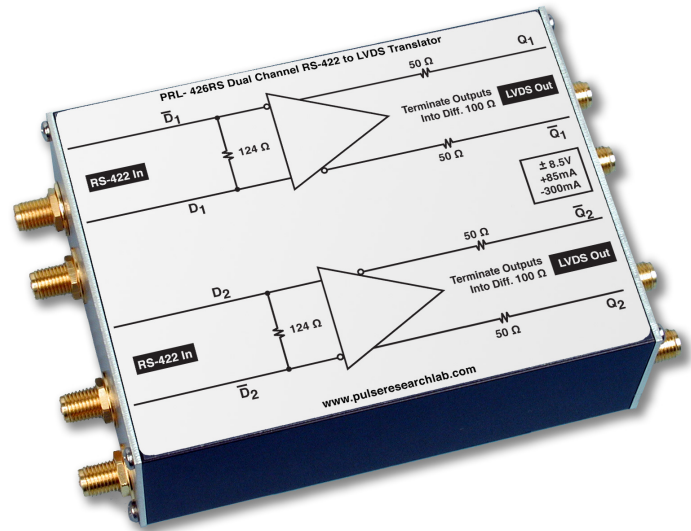
PRL-426RS DUAL CHANNEL RS-422 TO LVDS TRANSLATOR

APPLICATIONS

- Converting RS-422 Signals to LVDS Signals
- High Speed Digital Communications systems Testing
- High Speed SONET Clock Level Translation

FEATURES

- $f_{MAX} > 500$ MHz
- 1 ns Typical Output Rise & Fall Times
- Floating 124 Ω RS-422 Inputs
- Differential 50 Ω LVDS Outputs
- SMA I/O Connectors
- Self-contained 1.3 x 2.9 x 3.9-in. unit includes ± 8.5 V/1.4A AC/DC Adapter



PRL-426RS, RS-422 to LVDS Translator

DESCRIPTION

The PRL-426RS is a RS-422-to-LVDS Logic Level Translator. The differential outputs are 50 Ω back-terminated and are designed for driving floating 100 Ω loads, normally the configuration used in LVDS input circuits. The output swing is typically 600 mV with a common mode voltage of 1.2 V. These high speed translators facilitate testing of high speed digital communications circuits where conversion of RS-422 clock and data signals to LVDS signals is often required.

The inputs of the PRL-426RS consist of two pairs of SMA connectors, each internally terminated with 124 Ω between the two signal pins. The SMA shields are tied to chassis ground. They are designed to interface with the 124 Ω differential Serial Data/ $\overline{\text{Data}}$ or Clock/ $\overline{\text{Clock}}$ outputs from data communications equipment.

The standard unit has SMA input and output connectors. Model PRL-426RSTR has SMA input connectors and Triax output connectors. Model PRL-426RSTRI has Triax input connectors and SMA output connectors.

Each unit is supplied with a ± 8.5 V/1.4 A AC/DC Adaptor and housed in a 1.3 x 2.9 x 3.9-in. extruded aluminum enclosure. Available accessories include voltage distribution modules and brackets for mounting multiple units

*SPECIFICATIONS (0 °C ≤ T_A ≤ 35 °C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into floating 100 Ω loads.

SYMBOL	PARAMETER	PRL-426RS			UNIT
		Min	Typ	Max	
R_{IN}	Input Resistance	122	124	126	Ω
R_{INC}	Common Mode Input Resistance		5k		Ω
V_{CM}	Input Common Mode Voltage	-2.0		+3.0	V
R_{OUT}	Output Resistance	49.5	50.0	50.5	Ω
V_{OL}	Output Low Level		0.9		V
V_{OH}	Output High Level		1.5		V
V_{CMV}	Common mode voltage ¹		1.2		V
I_{DC}	DC Input Current		85 -265	100 -300	mA
V_{DC}	DC Input Voltage	±7.5	±8.5	±12	V
V_{AC}	AC/DC Adapter Input Voltage	103	115	127	V
t_{PLH}	Propagation Delay to output ↑		2		ns
t_{PHL}	Propagation Delay to output ↓		2		ns
t_{R/tr}	Rise/Fall Times (10%-90%) ²		1	1.25	ns
t_{SKEW}	Skew between any 2 outputs ³		200	500	ps
f_{MAX}	Max Clock Frequency ⁴	500	625		MHz
	Size	1.3 x 2.9 x 3.9			in.
	Weight	7			Oz

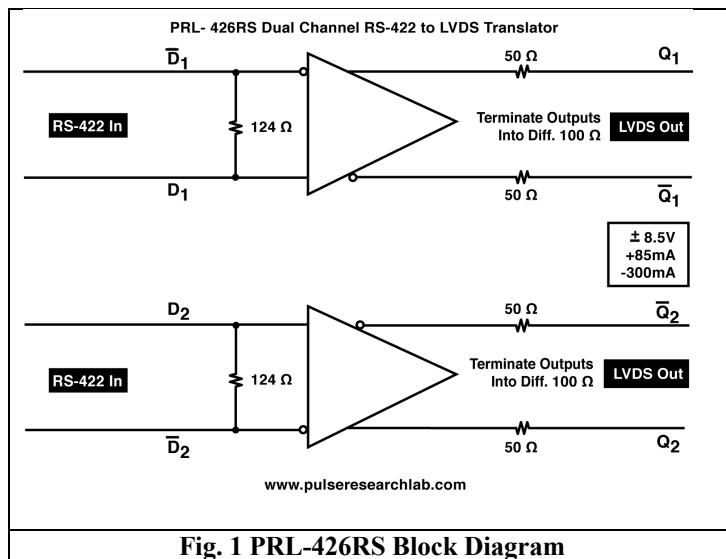


Fig. 1 PRL-426RS Block Diagram

Notes:

- (1) $V_{CMV} = (V_{OH} - V_{OL})/2$
- (2) Rise and Fall times are measured with SMA output connector units only and with ground-referenced 50 Ω loads.
- (3) Skew is measured at the output of a PRL-425N when driven by a PRL-426RS
- (4) f_{max} is measured using a PRL-425N with the corresponding input connectors as the receiver. The outputs of the PRL-425N are measured.