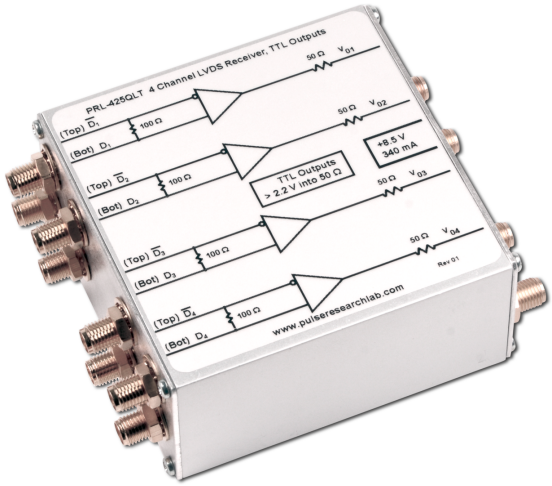
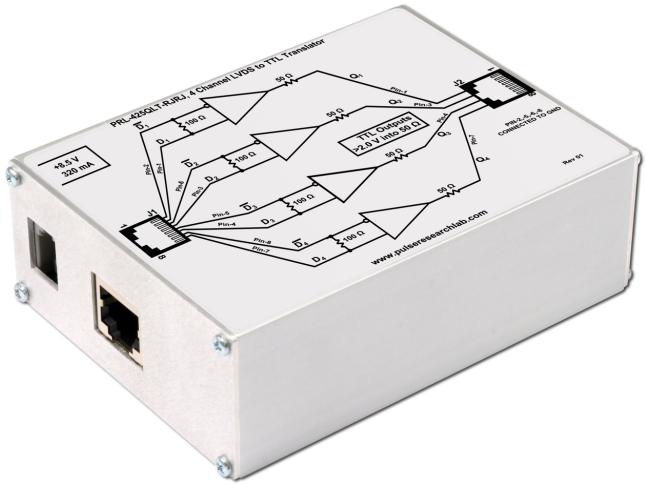
PRL-425QLT, FOUR CHANNEL LVDS TO TTL TRANSLATOR



PRL-425QLT-SMA, 4-Channel LVDS Receiver, 50 Ω TTL Outputs, SMA I/Os



PRL-425QLT-RJRJ, 4-Channel LVDS Receiver, 50 Ω TTL Outputs, RJ45 I/Os

APPLICATIONS

- LVDS to TTL Logic Level Translation
- Conversion of Differential Signals Transmitted through Long Lines to Single-Ended TTL Signals
- Mini Modular Instrument for interfacing with High Speed Data Communications Equipment

FEATURES

- 100 MHz Typical Maximum Clock Rate
- Floating 100 Ω Differential Inputs Accept LVDS or source-biased LVPECL Inputs
- 4 Single-Ended 50 Ω Back-Terminated TTL Outputs deliver 2.5 V into 50 Ω or 5 V into Hi-Z typical
- SMA or RJ45 I/O Connectors
- Single Supply, +7.5 VDC to +12 VDC, operation
- Ready-to-Use 1.3 x 2.9 x 2.9-in. or 3.9-in Module includes a ±8.5 V/1.8 A AC/DC Adapter

DESCRIPTION

The PRL-425QLT is a four channel LVDS receiver with single-ended 50 Ω TTL output line drivers. It is intended for converting differential signals transmitted through long lines into single-ended TTL outputs. The floating 100 Ω inputs are designed to be compatible with LVDS or source-biased LVPECL differential input signals. The 50 Ω back-terminated TTL output line drivers can drive long lines with or without terminations, and they are designed specifically for use with high speed data communication applications. Fig. 1 shows the standard LVDS input configuration. Functional block diagrams are shown in Figs. 2-3.

A feature of the TI DS90LV12A receiver chip in the PRL-425QLT is a "fail safe" state that sets the output logic Hi (TTL True) if the inputs are at the same voltage, which occurs if the inputs are left to float open or if they are shorted to GND. If this is undesired in your application, please consider the PRL-425T, 2 Ch. Universal Differential Receiver with TTL Outputs.

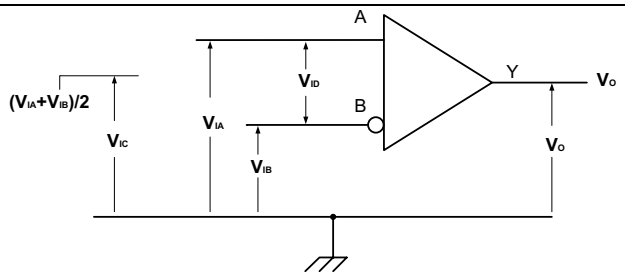


Fig. 1: LVDS Driver Block Diagram

Each PRL-425QLT is supplied with a ±8.5 V/1.8 A AC/DC Adapter, but it can also operate from a single positive power supply in the range of +7.5 V to +12 V.

The PRL-425QLT-SMA has SMA I/Os and is housed in a 1.3 x 2.9 x 2.9-in. extruded aluminum enclosure, while the PRL-425QLT-RJRJ has RJ45 I/Os and a length of 3.9-in. A future model, PRL-425QLT-RJS, will have an RJ45 input and SMA outputs.

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*SPECIFICATIONS (0° C ≤ T_A ≤ 35° C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into 50 Ω

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comment
R_{inD}	Differential Input Resistance		100		Ω	
R_{inC}	Common Mode Input Resistance		5K		Ω	
I_{DC1}	DC Input Current @ 50MHz		265	280	mA	
I_{DC2}	DC Input Current @ 85MHz		340	360	mA	
V_{ID}	Differential Input(1)	0.05	0.2	3	V	
V_{IA} or V_{IB}	Single ended input(1)	-0.3		3.9	V	
VCM	Common Mode Input(1)	0		3		
V_{DC}	DC Input Voltage	7.5	8.5	12	V	
V_{AC}	AC/DC Adapter Input Voltage	103	115	127	V	
V_{OHNL}	Output Hi Level, No Load	4.4	5.0		V	R_L=1 MΩ @ DC
V_{OHFL}	Output Hi Level, Full load	2.2	2.5		V	R_L=50 Ω @ DC
V_{OLNL}	Output Lo Level, No Load	-0.1	0	0.4	V	R_L=1 MΩ @ DC
V_{OLFL}	Output Lo Level, Full Load	-0.05	0.00	0.20	V	R_L=50 Ω @ DC
t_{PLH}	Propagation Delay to output ↑		2.2		ns	
t_{PHL}	Propagation Delay to output ↓		2.2		ns	
t_r/t_f	Rise/Fall Times		1.8	2.5	ns	PRL-425QLT-SMA
f_{max}	Max Clock Frequency	90	100		MHz	PRL-425QLT-SMA
t_{SKEW1}	Skew between outputs		250	600	ps	
DTY	Positive Duty Cycle @ 50MHz		55		%	
	Size		1.3 x 2.9 x 2.9		in.	PRL-425QLT-SMA
	Size		1.3 x 2.9 x 3.9		in.	RL-425QLT-RJRJ
	Weight		5		Oz	

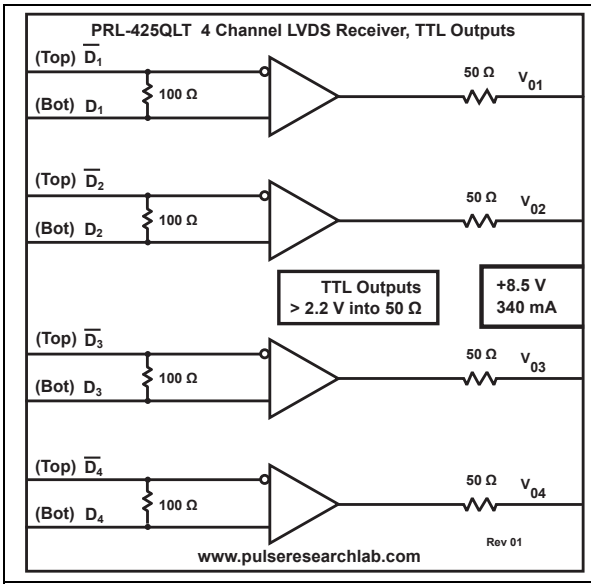


Fig. 2: PRL-425QLT-SMA Block Diagram

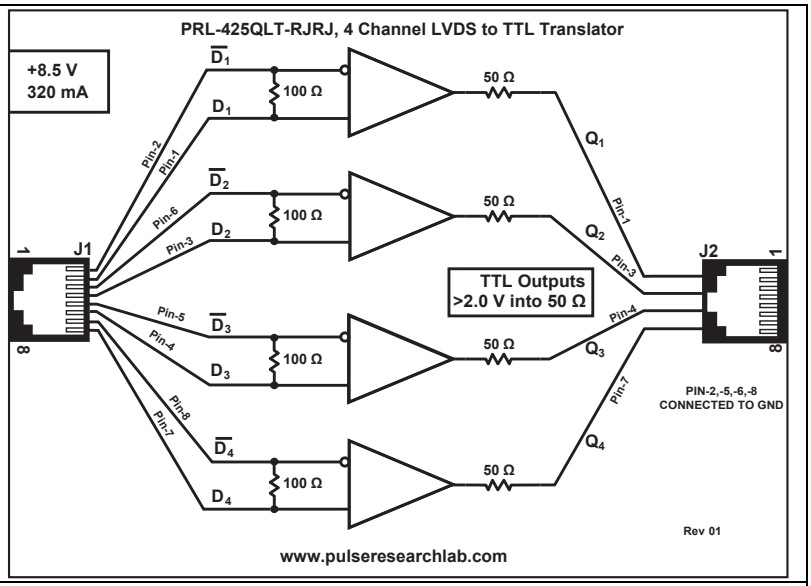


Fig. 3: PRL-425QLT-RJRJ Block Diagram

Notes:

(1) See Fig. 1

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