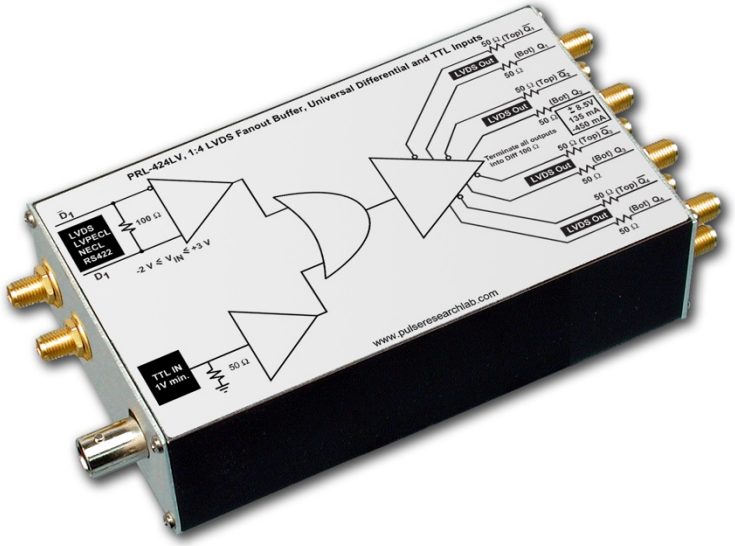
PRL-424LV 1:4 LVDS FANOUT BUFFER, UNIVERSAL DIFFERENTIAL AND TTL INPUTS

APPLICATIONS

- LVDS Fanout Buffer
- Converting Differential NECL/LVPECL/RS422 Signals to LVDS
- Converting TTL Signals to LVDS
- High Speed Digital Communications Systems Testing
- Satellite Telemetry/Ground Station System Integration



PRL-424LV

FEATURES

- f_{max} > 1.25GHz for LVDS/NECL/LVPECL inputs, > 300 MHz for TTL input
- 500 ps Typical Output Rise & Fall Times
- Floating 100 Ω Universal Differential Inputs Accept LVDS, LVPECL, NECL, or RS422 Inputs
- Separate TTL input (1 V minimum) Logically ORed with the Floating Differential Inputs
- 4 Pairs of Complementary 50 Ω LVDS Outputs
- SMA Connectors for LVDS/LVPECL/NECL Inputs, BNC Connector for TTL Input
- SMA Output Connectors
- Self-contained 1.3 x 2.9 x 5-in. unit includes ±8.5V/1.4A AC/DC Adapter

DESCRIPTION

The PRL-424LV is a 1:4 fanout, complementary output, LVDS line driver. It has a floating 100 Ω universal differential input suitable for accepting LVDS, LVPECL, NECL, or RS422 signals. It also has a logically ORed, 50 Ω TTL input with a minimum 1 V triggering threshold. The PRL-424LV high speed fanout line driver facilitates testing of high speed digital communications circuits and distribution of satellite signals.

The floating differential input accepts differential LVDS, LVPECL, NECL, RS422, or any 75 mV minimum differential signal within the window of -2.0 V to +3.0 V (option -01 has an input voltage range from -2.4 V to +4.0 V, and will accept 5 V PECL signals). When driven by LVPECL or NECL inputs, these signals must have internal 150 Ω or 200 Ω pull down resistors, respectively. The PRL-424LV differential input is compatible with all LVPECL or NECL output signals from the PRL family of products. The connectors for the universal differential input are SMA, and the connector for the TTL input is BNC. All output connectors are SMA.

The four pairs of complementary outputs are 50 Ω back-terminated and are designed for driving floating 100 Ω loads, normally the configuration used in LVDS input circuits. The output swing is typically 600 mV with a common mode voltage of 1.2 V.

The PRL-424LV is supplied with a ±8.5 V/1.4 A AC/DC adapter and housed in a 1.3 x 2.9 x 5-in. extruded aluminum enclosure. Available accessories include voltage distribution modules and brackets for mounting multiple units.

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*SPECIFICATIONS (0^0 C ≤ T_A ≤ 35^0C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into floating 100 Ω loads.

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comment
R_{in}	Differential Input Resistance	99	100	101	Ω	
R_{inC}	Common Mode Input Resistance		5k		Ω	
R_{out}	Output Resistance	49.5	50.0	50.5	Ω	
Vin	Input Voltage Range Option -01 Input Voltage Range	-2.0 -2.4		+3.0 +4.0	V	
V_{OL}	Output Low Level		0.9		V	
V_{OH}	Output High Level		1.5		V	
V_{CMO}	Output Common mode voltage[1]		1.2			
I_{DC}	DC Input Current		130 -370	140 -380	mA	
V_{DC}	DC Input Voltage	±7.5	±8.5	±12	V	
V_{AC}	AC/DC Adapter Input Voltage, 120 AC/DC Adapter Input Voltage, 220	103 206	115 220	127 254	V	
t_{PLH}	Propagation Delay to output ↑		2.7		ns	
t_{PHL}	Propagation Delay to output ↓		2.7		ns	
t_r/t_f1	Rise/Fall Times (10%-90%)[2]		500	650	ps	@200 MHz
t_r/t_f2	Rise/Fall Times (10%-90%)[2]		250		ps	@1.25 GHz
t_{SKEW}	Skew between any 2 outputs		200	550	ps	
f_{max}	Max Clock Frequency, SMA Input[3] Max Clock Frequency, TTL Input	1.25	1.35 300		GHz MHz	
	Size	1.3 x 2.9 x 5.0			in.	
	Weight	8			Oz	

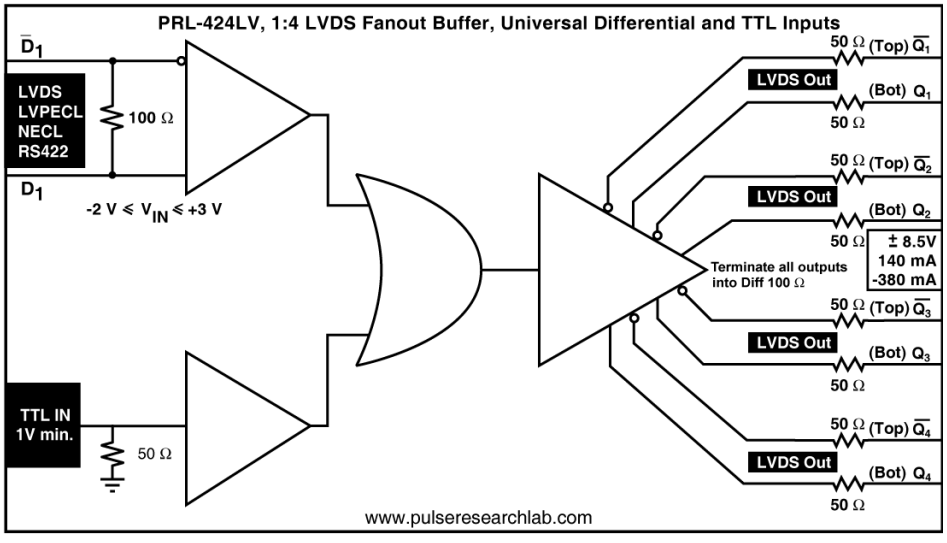


Fig. 1 PRL-424LV Block Diagram

Notes:
(1) $V_{CMVO} = (V_{OH}+V_{OL})/2$
(2) Rise and Fall times are measured with ground-referenced 50 Ω loads.
(3) f_{max} is measured using the PRL-174ANT Clock Driver outputs as the driver and the PRL-425N with SMA input connectors as the receiver. The outputs of the PRL-425N are measured. f_{max} for the TTL input is currently limited by the lack of TTL drivers faster than 300 MHz.

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